

Faculty of Engineering & Technology

Logic Design

Information :						
Course Code :	EED220	Level	:	Undergraduate	Course Hours :	3.00- Hours
Department : Biomedical Engineering						
Description :						
and standard for Minimization, an	binary numbers, and c rms, and digital logic g the map method for nalvsis procedure, desig	ates and the simplificatio	eir in n an	tegrated circuits. Gate dimplementation. Cor	-Level mbinational	

logic circuits: Analysis procedure, design procedure, binary adder. subtractor, binary multiplier, magnitude comparator, decoders, encoders, and multiplexers. Sequential logic circuits: Latches and Flip-Flops, analysis of clocked sequential circuits, and design procedure. Registers, counters, Memory, memory decoding, and programmable devices. Selected applied design examples with standard integrated circuits (ICs).